Electronic Version
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Claims

[c1] 1. A cell library for use in designing integrated domino circuits, comprising:
a first library portion including a plurality of FET logic circuits of first conductivity type to provide at least selectable transistor sizes;
and a second library portion including a plurality of selectable prechargeable complementary FET driver circuits, each configured to be connectable to an output of a selected one of said logic circuits, to provide at least selectable transistor sizes.

[c2] 2. The library of claim 1 wherein said logic circuits are n-FET logic circuits.

[c3] 3. The library of claim 1 wherein said logic circuits are p-FET logic circuits.

[c4] 4. The library of claim 1 wherein said complementary FET driver circuits are CMOS driver circuits.

[c5] 5. The library of claim 1 wherein said logic circuits are inverting logic circuits.

[c6] 6. The library of claim 1 wherein said driver circuits have

an inverting function.

[c7] 7. The library of claim 6 wherein at least some of said driver circuits are inverters.

[c8] 8. The library of claim 6 wherein at least some of said driver circuits comprise NOR gates.

[c9] 9. The library of claim 6 wherein at least some of said driver circuits comprise NAND gates.

[c10] 10. The library of claim 6 wherein at least some of said driver circuits are static driver circuits.

[c11] 11. The library of claim 1 wherein said driver circuits are selectable to match at least a size characteristic of said selected one of said logic circuits.

[c12] 12. The library of claim 1 further comprising at least selectable PMOS transistor connectable to said logic circuits to precharge elements thereof.

[c13] 13. The library of claim 1 wherein said logic circuits further comprise a footer circuit to disconnect said selected logic circuit from a pull-down potential during a precharge clock phase.

[c14] 14. The library of claim 1 further comprising a keeper circuit attached to an output of said logic circuit to hold

a precharge voltage thereon.

[c15] 15. The library of claim 1 wherein said MOS logic circuits are NMOS logic circuits.

[c16] 16. A cell library for use in designing integrated circuits, comprising:
a first library portion containing a plurality of NMOS logic circuits to provide selectable logic functions and transistor sizes;
and a second library portion containing a plurality of selectable driver circuits, each configured to be connectable to an output of a selected one of said logic circuits, said driver circuits being selectable to match at least a size characteristic of said selected one of said logic circuits.

[c17] 17. The library of claim 16 wherein said logic circuits are inverting logic circuits.

[c18] 18. The library of claim 17 wherein said driver circuits have an inverting function.

[c19] 19. The library of claim 18 wherein at least some of said driver circuits are inverters.

[c20] 20. The library of claim 18 wherein at least some of said driver circuits comprise NOR gates.

[c21] 21. The library of claim 18 wherein at least some of said driver circuits comprise NAND gates.

[c22] 22. The library of claim 18 wherein at least some of said driver circuits are static driver circuits.

[c23] 23. The library of claim 22 wherein at least some of said static driver circuits comprise a keeper circuit configured to hold a precharge value on an output of said logic circuit until an evaluate phase occurs.

[c24] 24. The library of claim 16 further comprising at least selectable PMOS transistor connectable to said logic circuits to precharge elements thereof.

[c25] 25. The library of claim 24 wherein said at least one PMOS transistor comprises a plurality of PMOS transistors of various selectable sizes.

[c26] 26. The library of claim 16 further comprising a selectable latch circuit connectable to said selected logic circuit to selectively maintain a logic value contained in said selected logic circuit.

[c27] 27. A cell library, comprising:
a plurality of selectable inverting NMOS logic circuits;
and a plurality of selectable inverter circuits, connectable to receive at least one output from a selected NMOS logic

circuit.

[c28] 28. The cell library of claim 27 wherein at least one of said inverter circuits has a plurality of inputs to which outputs of a corresponding plurality of said logic circuits are selectively connectable.

[c29] 29. The cell library of claim 27 wherein at least on of said NMOS logic circuits has an "AND" function.

[c30] 30. The cell library of claim 27 wherein at least on of said NMOS logic circuits has an "OR" function.

[c31] 31. The cell library of claim 27 wherein at least on of said NMOS logic circuits has a complex logic function including both "AND" and "OR" functions.

[c32] 32. The cell library of claim 27 wherein at least one of said inverter circuits is configured as a keeper circuit selectively connectable to said selected NMOS logic circuit.

[c33] 33. The cell library of claim 32 wherein said keeper circuit comprises:
a pair of PMOS devices and an NMOS device,
said NMOS device and one of said PMOS devices being connected to form an inverter circuit connectable to an output of said NMOS logic circuit;
and another of said PMOS devices being connected to re-

ceive an output of said inverter circuit and connectable to said output of said NMOS logic circuit to latch an existing state therein.

[c34] 34. A method for constructing an integrated circuit, comprising:
selecting a logic circuit from a cell library containing a plurality of logic circuits;
selecting a driver circuit from said cell library containing a plurality of driver circuits for connection to said selected logic circuit to match at least a size characteristic of said selected logic circuits.

[c35] 35. The method of claim 34 wherein said selecting a logic circuit comprises selecting an NMOS logic circuit.

[c36] 36. The method of claim 35 further comprising constructing a PMOS transistor for connection to said selected logic circuit to precharge same in a domino logic circuit.

[c37] 37. The method of claim 34 further comprising selecting a keeper circuit that inverts an output from said selected NMOS circuit and latches a logic value therein.